Octave Tunable, Highly Linear, RC-Ring Oscillator with Differential Fine-Coarse Tuning, Quadrature Outputs and Amplitude Control for Fiber Optic Transceivers

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Abstract — **This paper presents a low-voltage, RC-ring oscillator for fiber optic transceivers (SDH/SONET applications). It has one octave coarse tuning range, differential tuning inputs, quadrature outputs and a linear fine-control. A replica biasing circuit regulates the common-mode voltage and the amplitude at the output. The oscillator has been realized in a pre-production 70GHz f_T, SiGe, BiCMOS process (QUBIC4G). The tuning range covered with process and temperature variations is 3.4GHz-6.8GHz. At 6.6GHz oscillation frequency the measured phase noise is –92dBc/Hz @ 3MHz offset from the carrier. The typical power consumption of the VCO core is 80mW from a 2.5V power supply and the area is 0.3mm^2.**

I. INTRODUCTION

The advent of fiber optic communications has brought fully integrated optical receivers in which the quest for low power is of increasing importance at higher integration densities. At the receiver side, Data and Clock recovery units (DCR), PLL based, are needed to recover the clock information and to retime the incoming DATA [1-3]. Figure 1 shows a DCR, based on a Master-Slave approach. This principle relies on matched oscillators and two control loops for frequency and phase acquisition respectively. In a DCR, a possible choice would be a RC-ring oscillator due to its superior tuning range, linearity and the possibility of having quadrature outputs, mandatory for some applications. The disadvantages are the power consumption and its phase noise. When the data rate at the input has any value (any-rate) within a well-determined interval, e.g. 155Mb/s...2.5Gb/s, a large tuning range oscillator is required [3-5]. The linearity of the oscillator is also important for the reason of keeping the loop bandwidth of the PLL constant for different tuning frequencies. An octave tunable RC oscillator can generate any frequency below its oscillation frequency by frequency division, without the need for complicated frequency dividers. The aim of this paper is to show that one can achieve an octave tuning range with RC ring type oscillators with low phase noise by taking advantage of

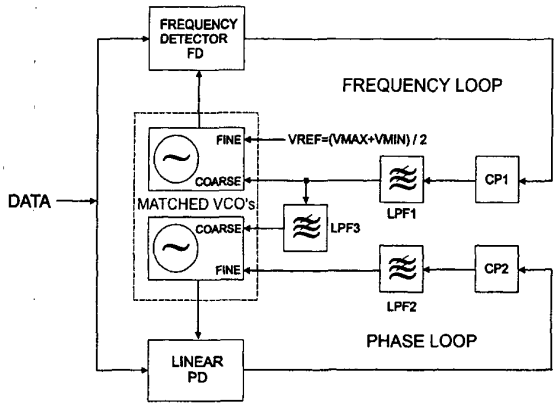

Fig. 1. DATA and clock recovery (DCR)

temperature and process variations compensation techniques. The design has been realized in a 70GHz f_T, SiGe, BiCMOS process (QUBIC4G).

II. CIRCUIT PRINCIPLE

A minimal differential ring oscillator (fig.2) consists of two inverters (gain stages) that each provide a delay t_D at the oscillation frequency. In order to satisfy the phase oscillation condition around the loop, it can be shown that the frequency of operation is given by:

$$f_0 = \frac{1}{4 t_D} \quad (1)$$

In order to obtain a high oscillation frequency in the GHz range, an obvious choice would be to limit the number of stages to the minimum (two). By changing the delay per stage the oscillation frequency will change. Fig.3 shows the basic building blocks of the inverter. A gain stage

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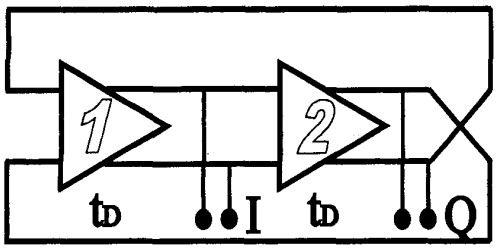

Fig. 2. Ring oscillator principle

amplifies the input differential voltage and has a load consisting of a positive resistor 2R and a negative resistor RTUNE. In order to provide a level shifting operation and to minimize the loading effect of the next stage a buffer has been included. The main time constant in the oscillator consists of the parallel combination of the positive and negative resistor and the parasitic capacitance "seen" in parallel by the resistive load. Tuning the negative resistance, the delay per stage will change and therefore the oscillation frequency will change too. By tuning the positive resistance 2R, two-tuning mechanisms are present.

Fig.4 shows the implementation of the gain stage and the buffer. The gain stage consists of a differential pair with load R and RTUNE, followed by an emitter follower with a MOS controlled current source. The MOS transistors in the buffer provide feed-forward control at the output. Due to this configuration, the gain of the buffer is slightly higher than 1dB but the main advantage consists of the fact that the buffer stage is able to deliver more current to a capacitive load. Therefore, slewing effects at the output can be reduced. In normal emitter followers, the constant current source in the emitter generates unequal rise and fall times. In an oscillator, this translates in non-symmetrical waves at the output that can worsen the phase noise. Since this oscillator provides sinusoidal, symmetrical waveforms at the output, the 1/f noise corner in the phase-noise spectrum is pushed towards the carrier minimizing the close-in phase noise of the oscillator. Also the noise coming from the down-conversion mechanism is reduced. On the other hand, if the amplitude of oscillation becomes to high, a normal emitter follower buffer can cause distortion when the output current source enters saturation.

The MOS transistor has the advantage that going from

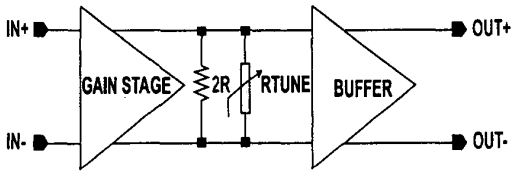

Fig.3: Basic building blocks in the ring oscillator

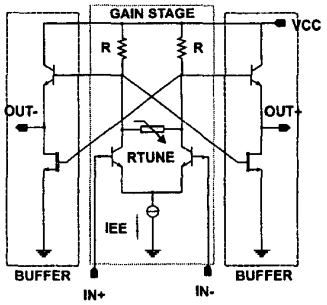

Fig.4: Inverter implementation

saturation into linear region, the output resistance changes gradually with reduced distortion of the output waveform.

The negative resistance implementation is shown in fig.5. Here, the transistors Q3 and Q4 work as a latch and in order to minimize the capacitive loading on the collector side, their bases are connected to the outputs OUT- and OUT+. The COARSE control has been implemented differentially using a parallel connection of a NMOS and a PMOS transistor (M1, M3 and M2, M4 respectively). The net load of the gain stage consists of a fixed resistor R in parallel with a differentially tunable MOS resistor and the differentially tunable negative resistance realized with the latch Q3-Q4. The FINE-control tuning is realized by using a differential voltage at the fine-tuning port VFINE+ and VFINE- converted into a differential current (IFINE) by the series resistors connected in the emitters of Q1,Q2 and Q3,Q4 respectively. The negative resistance of the latch changes with the FINE tune current as:

$$\mathbf{RTUNE} = -\frac{2}{g_m} = -\frac{4V_T}{I_{EE} \pm I_{FINE}} \qquad (2)$$

This provides a fine tuning mechanism with high linearity. Denote R_{TOT} the parallel combination of the resistor R and the equivalent resistance of the MOS combination M1, M3

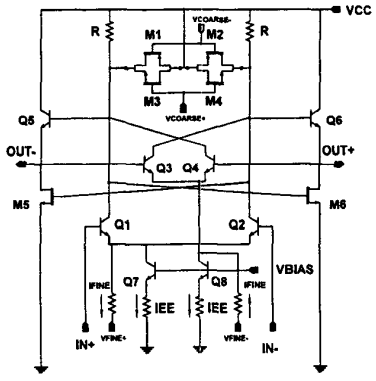

Fig.5: Realization of the negative and positive resistance

and M2, M4 respectively. Denote C_{PAR} the parasitic capacitance parallel with R_{TOT}. In a first order approximation, the oscillation frequency is given by:

$$f_0 \cong \frac{1}{4R_{TOT}C_{PAR}} - \frac{I_{EE}}{8V_T C_{PAR}}\left(1 \pm \frac{I_{FINE}}{I_{EE}}\right) \quad (3)$$

The coarse-tuning has a larger gain constant and allows one octave COARSE tuning of the oscillation frequency by modifying R_{TOT} via V_{COARSE}. In normal situations temperature and process variations will impair the constant swing at the output of the oscillator. That is why, in order to keep the same voltage swing in a large tuning range, we have to make sure that the net current flowing into the load times the net resistance present at the same node remains constant with respect to temperature, process variations and tuning. This can be realized with a replica bias circuit as depicted in fig.6. The replica bias is a one to one copy of the bias condition of the gain stage. The common-mode voltage at the two outputs OUT+ and OUT- is sensed by using two resistors and generates the voltage VCOMMON. The replica biasing tracks the temperature and process variations of the gain stage and latch circuit.

Let r_{bb}' denote the intrinsic base resistance of Q1 and Q2 and q the electron charge. The phase noise of the oscillator at f_m spacing from the carrier is given below [6]:

$$L(f_m) \cong 10\log\left\{\frac{q}{2I_{EE}\ln 2}\left(\frac{f_0}{f_m}\right)^2\left[\frac{1}{2} + \frac{V_T}{I_{EE}R_E} + \frac{r_{bb}'}{3R_{TOT}} + \frac{7V_T}{I_{EE}R_{TOT}}\right]\right\} \quad (4)$$

By increasing the current consumption (I_{EE}) and/or increasing the products $I_{EE}R_E$ & $I_{EE}R_{TOT}$ one can reduce the phase noise of the oscillator. This obviously conflicts with the low-power / low supply / high oscillation frequency requirements and octave tuning requirement.

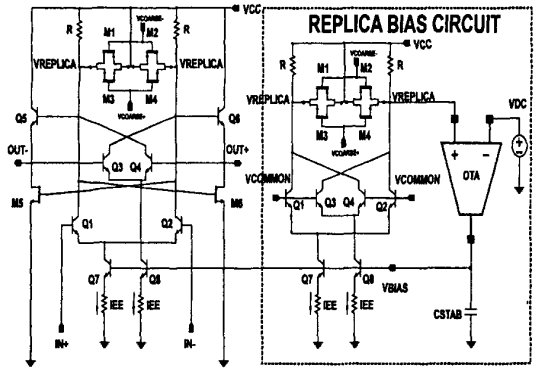

Fig.6: Inverter + replica biasing stage

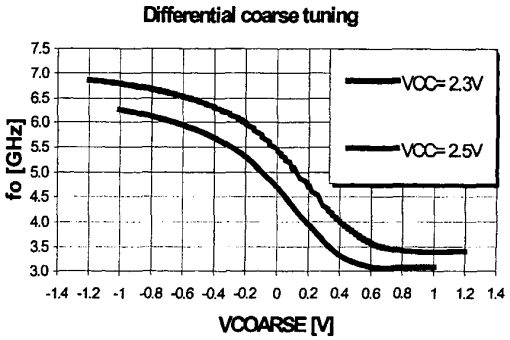

Fig.7: COARSE tuning curve @ VREPLICA=2.3V

III. MEASUREMENT RESULTS

Fig.7 presents the measured COARSE tuning characteristics for two different supply voltages: nominal 2.5V and 2.3V. It shows the octave range of the ring VCO and the low-voltage properties of the design. As predicted by eq. (3), the tuning curve is nonlinear. Fig.8 depicts the fine tuning curve for a common-mode voltage at COARSE inputs of VCOARSE=VCC/2=1.25V. Again, as predicted by eq. (3), we have a highly linear control with a gain of about 50MHz/Volt proven beneficial in order to decrease the sensitivity of the VCO with respect to external factors. The linearity of the tuning characteristic ensures a constant PLL bandwidth with respect to the fine tuning mechanism used in the phase control loop. The measured power at the two outputs changes with only 1dB in the whole COARSE interval. Phase noise measurements based on closed-loop PLL measurement set-up (HP3048A) are impaired by the high sensitivity (>1GHz/V) of the oscillator with respect to the COARSE tuning and the limited FM modulation of our generator. The phase noise measurement based on the

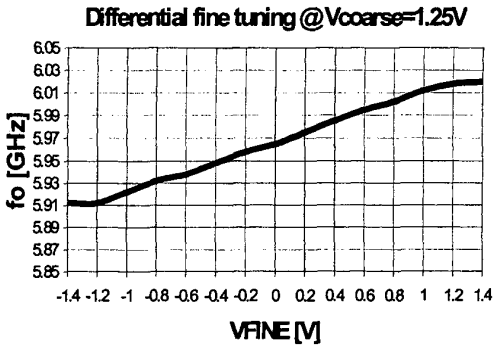

Fig.8: FINE tuning curve @VCOARSE(CM)=1.25V

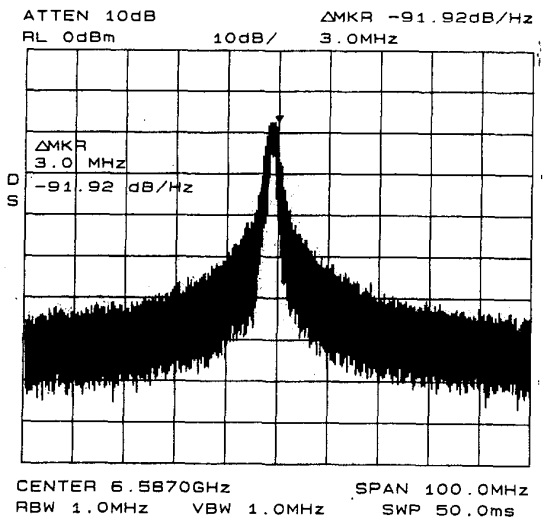

Fig.9: VCO spectrum and phase-noise @ 6.6GHz

spectrum analyzer are shown in fig.9. Here, the spectrum of the VCO at 6.6GHz oscillation frequency is presented.

The measured phase noise at 3MHz (ΔMKR) from the carrier is –92dBc/Hz pointing out the need for a larger PLL bandwidth when compared to a LC type VCO [7]. The phase noise varies only 2dB in the whole tuning range 3.4-6.8GHz. Fig.10 presents the chip photomicrograph where the place of the different building blocks is explicitly shown. The two buffers BUFF I and BUFF Q generate the quadrature signals I and Q. The differential swing is 800mVpp in a 50Ω, on-chip, load resistance. This was needed for measurement purposes. The inverters 3 and 4 are the ring inverters whilst the inverters 1 and 6 are the replica biasing circuits. Dummy inverters (2 and 5) have been included for symmetry reasons. To be remarked the perfect symmetry of the layout to keep the differential signal transfer properties of the circuit. The two OTA's are used in the replica biasing circuit. The power consumption of the inverters and OTA is 80mW from a 2.5V voltage supply and the chip area 0.3mm^2.

IV. CONCLUSIONS

We have presented an octave tunable RC oscillator with two differential tuning mechanisms. It works at 2.5V nominal supply and proves good performance down to 2.3V supply voltage. The fine tuning mechanism provides a highly linear tuning with 50MHz/Volt. A replica biasing circuit controls the common-mode and the oscillation amplitude providing temperature and process variations compensation. The measured phase-noise is –92dBc/Hz @

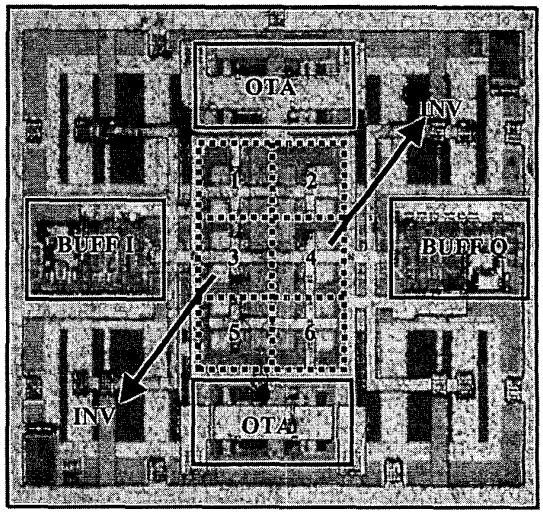

Fig.10: VCO chip photo

3MHz offset from the carrier and 6.6GHz oscillation frequency. The power consumption of the VCO core and the two OTA's is 80mW and the chip area is 0.3mm^2. It is realized in a 70GHz pre-production SiGe process.

ACKNOWLEDGEMENT

The authors wish to acknowledge the assistance of Marko van Houdt and Gilbert Gloaguen.

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